Customer No.: 31561
Application No.: 10/605,053
Docket No.: 9719-US-PA

## REMARKS

**Present Status of the Application**

The Office Action rejected claims 1-4, 12 and 14-15 under 35 U.S.C. 102(b), as being anticipated by Pinkham et al. (U.S. 5,646,896). The Office Action also objected claims 5-11, 13 and 16-21 as being dependent upon rejected based claims.

**Discussion of Office Action Rejections**

The Office Action rejected claims 1-4, 12 and 14-15 under 35 U.S.C. 102(b), as being anticipated by Pinkham et al. (U.S. 5,646,896). Applicant respectfully traverses the rejection for at least the reasons set forth below.

With respect to claim 1, as original filed, recites:

> Claim 1 (as original) A memory architecture used to repair a serial access memory comprising a main memory, a redundant memory and a control interface circuit, the control interface circuit storing a plurality of addresses, each of the addresses corresponding to a damaged memory cell in the main memory,
> when the memory module is accessed by an access address, the control interface circuit issuing a pointer address pointing to a corresponding address in the stored addresses in the control interface circuit and comparing the address corresponding to the pointer address and the access address. If the address corresponding to the pointer address is equal to the access address, data accessed by the access address from the memory module is read out from the redundant memory.

Applicant submits that such a memory architecture as set forth in claim 1 is neither taught, disclosed, nor suggested by Pinkham '896.

First of all, Pinkham '896 fails to disclose a memory architecture as set forth in claim 1. Although Pinkham '896 teaches both a random and a serial access memory (RAM and SAM) of a dual port memory device (Column 4, lines 25- 27), an independent repair of subarrays in dual port memory systems (Column 6, lines 44 and 45), a SAM control circuitry 22 (Column 3, line 26; element 22 in FIG. 1) as the Examiner stated corresponding to the elements as set forth in claim 1, Pinkham '896 does not teach a memory architecture composed of the foregoings. A memory architecture as set forth in claim 1 should have all elements compatible and incorporative to each other. Since Pinkham '896 teaches the listed elements either in the "Background of the Invention" or in different embodiments, rather than in an individual workable embodiment, the elements taught by Pinkham '896 are either not correspondingly equivalent to those as set forth in claim 1 or not adapted for composing a memory architecture as set forth in claim 1, that is the intrinsic relationship among the elements of the memory architecture as set forth in claim 1 that is required by the present invention is not discovered by Pinkham '896.

In details, with respect to the limitation of "when the memory module is accessed by an access address, the control interface circuit issuing a pointer address pointing to a corresponding address in the stored addresses in the control interface circuit and comparing the address corresponding to the pointer address and the access address", the Examiner indicates that it is taught by "a method for accessing a redundant address in a dual port memory device..." (Column 9, lines 40) combining with "The address received to access the SAM is compared with address

stored in the fuse bank. The fuse bank is pointed by the output of the counter (e.g., bits C0 and C1 shown in FIG. 2B)). However, the cited sentence of "a method for accessing a redundant address in a dual port memory device..." (Column 9, lines 40) as set forth in Pinkham '896 only discloses a method or a probability of accessing a redundant address in a dual port memory device. It is neither disclosed nor taught to be a corresponding condition to the latter "the control interface circuit issuing a pointer address pointing to a corresponding address in the stored addresses in the control interface circuit and comparing the address corresponding to the pointer address and the access address" which is required by the present invention as set forth in claim 1. Since there is no relationship between the foregoing two situation disclosed by Pinkham '896, Applicant submits that Pinkham '896 fails to disclose a limitation of "when the memory module is accessed by an access address, the control interface circuit issuing a pointer address pointing to a corresponding address in the stored addresses in the control interface circuit and comparing the address corresponding to the pointer address and the access address".

In a similar manner, with respect to claim 14, as original filed, recites:

> A method for repairing a serial access memory, the memory module comprising a main memory, a redundant memory and a control interface circuit, the control interface circuit for storing a plurality of addresses, each of the addresses corresponding to a damaged memory cell in the main memory,
> assessing the memory module by an access address;
> issuing a pointer address by the control interface circuit to point to a corresponding one of the stored addresses stored in the control interface circuit;
> comparing the address corresponding to the pointer address and the access address, if the address corresponding to the pointer address is equal to the access address, data accessed by the access address from the memory module being read out from the redundant memory.

Applicant submits that such a method for repairing a serial access memory as set forth in claim 14 is neither taught, disclosed, nor suggested by Pinkham '896.

Applicant submits that Pinkham '896 fails to disclose a step of "assessing the memory module by an access address" which is required by the present invention as set forth in claim 14. The Examiner cites "shared fuse programming circuitry, coupled to said first memory, for programming redundant addresses for said first memory" (column 9, lines 8-11; element 30 in FIG. 2). However, the cited part does not teach the foregoing step. As interpreted by the Examiner as set forth in the OFFICE ACTION, the word "programming" is equivalent to "storing" rather than "assessing". Therefore, Applicant submits that Pinkham '896 fails to disclose the step of "assessing the memory module by an access address".

Furthermore, Pinkham '896 fails to disclose a workable sequence of the steps cited by the Examiner which is also required by the present method for repairing a serial access memory.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 14 are submitted to be novel, unobvious, and patentable over Pinkham, and should be allowable. For at least the same reasons, dependent claims 2-4, 12 and 15 patently define over

the prior art as well. If the independent claims 1 and 14 are allowable, then claims 5-11, 13 and 16-21 as being dependent upon respectively claims 1 and 14 should also be allowable.

Applicant further submits that if any of claims 1 and 14 should be rejected on the grounds of a new prior art rejection in the next Office Action, that Action cannot be made FINAL, as such a rejection could not be considered to have been necessitated by amendment. MPEP §706.07(a)

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## CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-21 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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